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WORKED EXAMPLES

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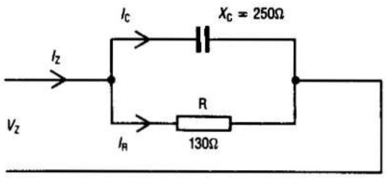
PART 1—Electrical and Electronic Principles IV (BTEC)

Q1 *A resistor of 130 Ω is connected in parallel with a capacitor whose reactance is 250 Ω at the frequency of the supply. The current flowing into the network is 20 mA.*

- (*a*) *Calculate the current flowing in each branch.*
- (*b*) *Find the phase angle between the supply current and voltage.*

A1



For the parallel circuit, by Pythagoras' theorem,

$$I_Z^2 = I_R^2 + I_C^2.$$

$$\therefore \quad \left(\frac{V_Z}{Z}\right)^2 = \left(\frac{V_Z}{R}\right)^2 + \left(\frac{V_Z}{X_C}\right)^2.$$

Dividing through by V_Z^2,

$$\frac{1}{Z^2} = \frac{1}{R^2} + \frac{1}{X_C^2}.$$

$$\therefore \quad \frac{1}{Z} = \sqrt{\left(\frac{1}{R^2} + \frac{1}{X_C^2}\right)} = \sqrt{\left(\frac{1}{130^2} + \frac{1}{250^2}\right)}\,\text{S}$$

$$= \sqrt{(59{\cdot}17 + 16)10^{-6}}\,\text{S} = 8{\cdot}67 \times 10^{-3}\,\text{S}.$$

$$\therefore \quad Z = \frac{1}{8{\cdot}67 \times 10^{-3}}\,\Omega = 115{\cdot}34\,\Omega.$$

$$V_Z = I_Z Z = 20 \times 10^{-3} \times 115{\cdot}34\,\text{V} = 2{\cdot}307\,\text{V}.$$

$$I_R = \frac{V_Z}{R} = \frac{2{\cdot}307}{130}\,\text{A} = \underline{17{\cdot}746\,\text{mA.}}$$

$$I_c = \frac{V_Z}{X_C} = \frac{2{\cdot}307}{250}\,\text{A} = \underline{9{\cdot}23\,\text{mA.}}$$

(*b*)

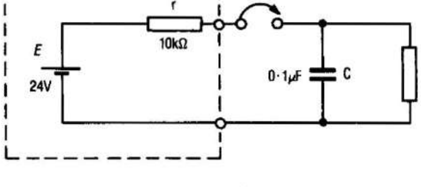
$$\theta = \tan^{-1}\frac{I_C}{I_R} = \tan^{-1}\frac{9{\cdot}23}{17{\cdot}746} = 27{\cdot}48°.$$

The supply current leads the supply voltage by $\underline{27{\cdot}5°}$.

Q2 *A capacitor of 0·1 μF is placed in parallel with a 5 kΩ resistor and the combination is then connected to a DC generator of internal resistance 10 kΩ and EMF 24 V.*

Calculate the potential difference across the capacitor 1 ms after the connection is made, given that the initial charge on the capacitor is zero.

A2



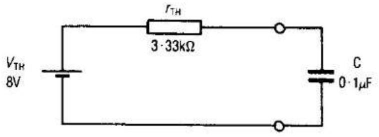
> From a practical point of view, it is obvious that the capacitor, which has no initial charge, will, at the moment of connection of the supply, begin to charge up towards a potential difference of 24 V. If the capacitor potential difference were to reach 24 V, no current would continue to flow through resistor r and then the capacitor would begin to discharge through resistor R. At some point, an equilibrium condition will be reached. This depends on the value of E and the voltage division between resistors r and R.
>
> The problem can be solved by finding the Thévenin equivalent circuit, where the capacitor becomes the load.

Ignoring the capacitor,

$$V_{\mathrm{TH}} = E\frac{R}{r+R} = 24\left(\frac{5}{5+10}\right)\,\mathrm{V} = 8\,\mathrm{V}.$$

When the DC generator is replaced by a short circuit, looking back from the output terminals, resistors R and r can be seen to be in parallel

$$\therefore \quad r_{\mathrm{TH}} = \frac{rR}{r+R} = \frac{10 \times 5}{10+5} \times 10^3\,\Omega = 3{\cdot}33\,\mathrm{k}\Omega.$$



The potential difference across the capacitor is given by the exponential charging formula

$$v_{\mathrm{c}} = V(1 - \mathrm{e}^{-t/\tau}),\text{ where } \tau = CR.$$

For the equivalent circuit, $\tau = Cr_{\mathrm{TH}}$ and $V = V_{\mathrm{TH}}$.

$$\therefore \quad \tau = 0{\cdot}1 \times 10^{-6} \times 3{\cdot}33 \times 10^{3}\,\mathrm{s} = 3{\cdot}33 \times 10^{-4}\,\mathrm{s}.$$

$$\frac{t}{\tau} = \frac{1 \times 10^{-3}}{3{\cdot}33 \times 10^{-4}} = 3.$$

$$\therefore \quad v_{\mathrm{c}} = 8(1 - \mathrm{e}^{-3})\,\text{volts} = \underline{7{\cdot}6\,\mathrm{V}}.$$

Q3 *A series circuit consists of a pure inductor of reactance 120 Ω and a resistor of 80 Ω.*

(*a*) *Calculate the equivalent parallel circuit.*

(*b*) *Find the admittance, conductance and susceptance of the circuit.*

(*c*) *Find the inductance of the inductor for each case and draw the equivalent circuits, when the supply frequency is 400 Hz.*

A3 (*a*) For the series circuit,

$$Z = R + \mathrm{j}X_{\mathrm{L}} = 80 + \mathrm{j}120\,\Omega.$$

$$\therefore \quad \frac{1}{Z} = \frac{1}{80 + \mathrm{j}120}\,\mathrm{S}.$$

Rationalizing,

$$\frac{1}{Z} = \frac{80 - \mathrm{j}120}{(80 + \mathrm{j}120)(80 - \mathrm{j}120)} = \frac{80 - \mathrm{j}120}{80^2 + 120^2} = \frac{80 - \mathrm{j}120}{20\,800}\,\mathrm{S},$$

$$= \frac{8}{2080} - \mathrm{j}\frac{12}{2080} = \frac{1}{260} - \frac{\mathrm{j}}{173{\cdot}3} = \frac{1}{260} + \frac{1}{\mathrm{j}173{\cdot}3}\,\mathrm{S}.$$

Comparing with the parallel form

$$\frac{1}{Z} = \frac{1}{R} + \frac{1}{\mathrm{j}X_{\mathrm{L}}},$$

gives $R = \underline{260\,\Omega}$, $X_L = \underline{173{\cdot}3\,\Omega}$. (These are the values for the parallel circuit.)

(*b*) From $\dfrac{1}{Z} = \dfrac{1}{260} + \dfrac{1}{\mathrm{j}173{\cdot}3}$ S.

$$\frac{1}{Z} = Y = (3{\cdot}846 - \mathrm{j}5{\cdot}77) \times 10^{-3}\ \mathrm{S}.$$

Comparing with the general form

$$Y = G + \mathrm{j}B,$$

$$G = \underline{3{\cdot}846 \times 10^{-3}\ \mathrm{S}} \qquad B = \underline{-5{\cdot}77 \times 10^{-3}\ \mathrm{S}.}$$

$$Y = \sqrt{(G^2 + B^2)} = \sqrt{(3{\cdot}846^2 + 5{\cdot}77^2)} \times 10^{-3} = \underline{6{\cdot}93 \times 10^{-3}\ \mathrm{S}.}$$

(*c*)

$$X_L = 2\pi f L.$$

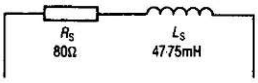
$$\therefore \quad L = \frac{X_L}{2\pi f}.$$

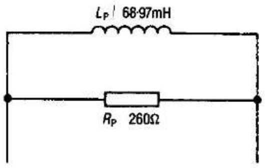
For the series inductor,

$$L_s = \frac{120}{2\pi \times 400}\ \mathrm{H} = \underline{47{\cdot}75\ \mathrm{mH}.}$$

For the parallel inductor,

$$L_p = \frac{173{\cdot}3}{2\pi \times 400}\ \mathrm{H} = \underline{68{\cdot}97\ \mathrm{mH}.}$$





Q4 *Figure 1 shows the circuit of a high-pass equaliser whose components are a capacitor of 68 nF and a resistor of 18 kΩ.*

(*a*) *Calculate the 3 dB frequency.*
(*b*) *Find the frequency at which the output is down by 4 dB.*

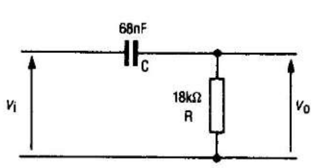


Figure 1

A4 (*a*) By voltage division,

$$\frac{v_o}{v_i} = \frac{R}{R + \dfrac{1}{\mathrm{j}\omega C}} = \frac{1}{1 + \dfrac{1}{\mathrm{j}\omega CR}} = \frac{1}{1 - \mathrm{j}\dfrac{1}{\omega CR}}.$$

When $\dfrac{1}{\omega CR} = 1$, $\dfrac{v_o}{v_i} = \dfrac{1}{1 - \mathrm{j}1}$.

$\therefore \quad \left|\dfrac{v_o}{v_i}\right| = \dfrac{1}{\sqrt{(1^2 + 1^2)}} = \dfrac{1}{\sqrt{2}}$, which gives the 3 dB condition

At the 3 dB frequency, $\frac{1}{\omega CR} = 1$.

$$\therefore \quad \omega = \frac{1}{CR}.$$

$$\therefore \quad f = \frac{1}{2\pi CR} = \frac{1}{2\pi \times 68 \times 10^{-9} \times 18 \times 10^{3}} = \underline{130\,\text{Hz.}}$$

(*b*)

$$\text{Gain} = 20 \log \frac{v_o}{v_i}\ \text{dB}.$$

$$\therefore \quad \frac{\text{Gain}}{20} = \log \frac{v_o}{v_i}.$$

$$\therefore \quad \frac{v_o}{v_i} = \text{antilog}\left(\frac{\text{gain}}{20}\right) = 10^{\text{gain}/20}.$$

When the output is 4 dB down,

$$\frac{v_o}{v_i} = 10^{-4/20} = 0{\cdot}63.$$

The circuit time constant, $\tau = CR$.

$$\therefore \quad \tau = 68 \times 10^{-9} \times 18 \times 10^{3} = 1{\cdot}224 \times 10^{-3}\ \text{s}.$$

Inserting the values for $\frac{v_o}{v_i}$ and τ into the equation of part (*a*),

$$\frac{v_o}{v_i} = \frac{1}{1 - \mathrm{j}\dfrac{1}{\omega CR}}.$$

$$\therefore \quad 0{\cdot}63 = \frac{1}{1 - \mathrm{j}\dfrac{1}{\omega 1{\cdot}224 \times 10^{-3}}}.$$

$$\therefore \quad 1 - \mathrm{j}\frac{1}{\omega 1{\cdot}224 \times 10^{-3}} = \frac{1}{0{\cdot}63}.$$

$$\therefore \quad 1 - \mathrm{j}\frac{1}{\omega 1{\cdot}224 \times 10^{-3}} = 1{\cdot}585.$$

$$\therefore \quad 1 - \mathrm{j}\frac{817}{\omega} = 1{\cdot}585.$$

At this point, it must be realised that the j term cannot be left on its own by transposing the '1'. In order to separate ω, the magnitude of the left hand side must be obtained.

$$\therefore \quad \sqrt{\left\{1 + \left(\frac{817}{\omega}\right)^2\right\}} = 1{\cdot}585.$$

$$\therefore \quad 1 + \left(\frac{817}{\omega}\right)^2 = 1{\cdot}585^2.$$

$$\therefore \quad \left(\frac{817}{\omega}\right)^2 = 1{\cdot}585^2 - 1.$$

$$\therefore \quad \frac{817}{\omega} = \sqrt{(1{\cdot}585^2 - 1)} = 1{\cdot}23.$$

$$\therefore \quad \omega = \frac{817}{1{\cdot}23} \text{ rad s}^{-1}.$$

$$\therefore \quad f = \frac{817}{2\pi \times 1{\cdot}23} = \underline{106 \text{ Hz.}}$$

Q5 The circuit shown in Figure 2 represents a top-cut tone control network connected to the output of an audio amplifier. The amplifier generates an EMF E and has an internal resistance, r, of 40 kΩ. For minimum top-cut the rheostat is set at its maximum value.

Calculate the loss at 15 kHz compared with that which occurs at 1 kHz. Express the loss in decibels.

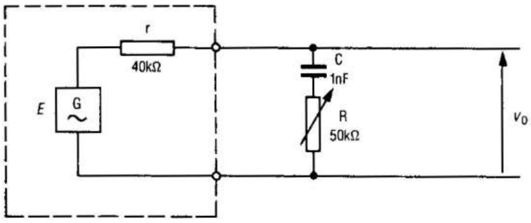


Figure 2

A5 By voltage division

$$\frac{v_o}{E} = \frac{R + \dfrac{1}{j\omega C}}{r + R + \dfrac{1}{j\omega C}}.$$

Multiplying numerator and denominator by $j\omega C$,

$$\frac{v_o}{E} = \frac{1 + j\omega CR}{1 + j\omega C(r + R)}.$$

At 15 kHz, when $R = 50\text{ k}\Omega$,

$$\omega CR = 2\pi \times 15 \times 10^3 \times 1 \times 10^{-9} \times 50 \times 10^3 = 4{\cdot}7.$$

Also, at 15 kHz,

$$\omega C(r + R) = 2\pi \times 15 \times 10^3 \times 1 \times 10^{-9} \times (40 + 50)10^3 = 8{\cdot}48.$$

$$\therefore \quad \frac{v_o}{E} = \frac{1 + j4{\cdot}7}{1 + j8{\cdot}48}.$$

Rationalizing,

$$\frac{v_o}{E} = \frac{(1 + j4{\cdot}7)(1 - j8{\cdot}48)}{1 + 8{\cdot}48^2} = \frac{40{\cdot}856 - j3{\cdot}78}{72{\cdot}9} = 0{\cdot}56 - j0{\cdot}052.$$

$$\therefore \quad \left|\frac{v_o}{E}\right| = \sqrt{(0{\cdot}56^2 + 0{\cdot}052^2)} = 0{\cdot}562 \qquad \text{at 15 kHz.}$$

At 1 kHz for the same setting of R, since the frequency is now $\frac{1}{15}$th of the value,

$$\omega CR = \frac{4{\cdot}7}{15} = 0{\cdot}313,$$

and

$$\omega C(r + R) = \frac{8{\cdot}48}{15} = 0{\cdot}565.$$

$$\therefore \quad \frac{v_o}{E} = \frac{1 + j0{\cdot}313}{1 + j0{\cdot}565}.$$

Rationalizing,

$$\frac{v_o}{E} = \frac{(1 + \mathrm{j}0{\cdot}313)(1 - \mathrm{j}0{\cdot}565)}{1 + 0{\cdot}565^2} = \frac{1{\cdot}177 - \mathrm{j}0{\cdot}252}{1{\cdot}319} = 0{\cdot}89 - \mathrm{j}0{\cdot}19.$$

$$\therefore \quad \left|\frac{v_o}{E}\right| = \sqrt{(0{\cdot}89^2 + 0{\cdot}19^2)} = 0{\cdot}91 \qquad \text{at 1 kHz.}$$

Comparing the two values of $\left|\frac{v_o}{E}\right|$,

$$\text{gain} = 20 \log \frac{0{\cdot}562}{0{\cdot}91} = 20 \log 0{\cdot}6176 = -4{\cdot}186\,\text{dB}.$$

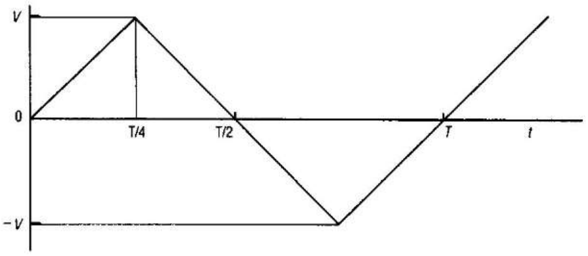
The gain has a negative value, so loss = $\underline{4{\cdot}186\,\text{dB}}$.

Q6 *A signal generator, calibrated in peak values is connected to a 1000 Ω heating element and the output voltage set at 8 V. By mistake, the function switch is set to triangular wave instead of sine wave.*

Calculate the percentage difference in heating which occurs because of the incorrect setting.

A6

> At first reading, this problem appears to be fairly straightforward. However, although the RMS value is easily obtained for the sine wave it is not so readily to hand for the triangular wave.
>
> To find the RMS value for the triangular wave, the equation of the wave must be set up, after which it must be squared, its mean value obtained and the process completed by taking the square root.



The waveform may be considered over one quarter cycle.

The equation for a straight line is

$$y = mx + C,$$

where m is the gradient.

In this case, $C = 0$ and $x = t$ while $y = v$.

$$\therefore \quad v = mt.$$

Taking m over the first quarter cycle where T is the periodic time

$$m = \frac{V}{T/4} = \frac{4V}{T}.$$

$$\therefore \quad v = \frac{4V}{T} t.$$

Taking the square of the voltage

$$v^2 = \left(\frac{4V}{T}\right)^2 t^2,$$

where $\left(\frac{4V}{T}\right)^2$ is a constant for a given triangular wave.

Obtaining the mean squared value (MSV) by integration,

$$\text{MSV} = \frac{1}{T/4}\int_0^{T/4}\left(\frac{4V}{T}\right)^2 t^2\,\mathrm{d}t.$$

Removing the constant from the integral and rearranging,

$$\text{MSV} = \frac{64V^2}{T^3}\int_0^{T/4} t^2\,\mathrm{d}t = \frac{64V^2}{T^3}\left[\frac{t^3}{3}\right]_0^{T/4} = \frac{64V^2}{3T^3}\left\{\left(\frac{T}{4}\right)^3 - 0\right\} = \frac{64V^2}{3T^3}\times\frac{T^3}{64} = \frac{V^2}{3}.$$

Taking the square root,

$$V_{\text{RMS}} = \frac{V}{\sqrt{3}}.$$

When the function switch is set to sine wave,

$$P = \frac{V_{\text{RMS}}^2}{R} = \frac{(8/\sqrt{2})^2}{1000}\ \text{W} = 32\ \text{mW}.$$

When the function switch is set to triangular wave,

$$P = \frac{(8/\sqrt{3})^2}{1000}\ \text{W} = 21{\cdot}33\ \text{mW}.$$

The difference in heating is given by

$$\frac{32 - 21{\cdot}33}{32}\times 100\% = \underline{33{\cdot}3\%.}$$

Q7 The tee attenuator shown in Figure 3 is said to correctly match a 600 Ω generator to its load. The values of resistors R1 and R2 are 360 Ω and 320 Ω, respectively. The generator EMF is 10 V.

(a) Confirm that the load is correctly matched to the generator.
(b) Find the attenuation produced by the tee network.
(c) Calculate the potential difference across the load when it is connected and the overall attenuation in decibels.

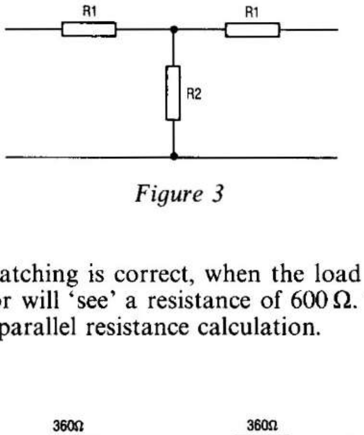
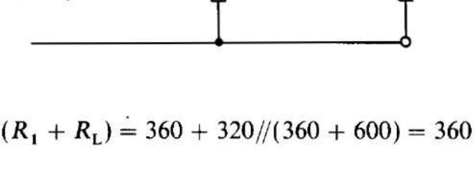


Figure 3

A7

If the matching is correct, when the load of 600 Ω is connected, the generator will 'see' a resistance of 600 Ω. This may be confirmed by a series-parallel resistance calculation.

(*a*)



$$R_0 = R_1 + R_2/\!/(R_1 + R_L) = 360 + 320/\!/(360 + 600) = 360 + \frac{320\times 960}{320 + 960}\ \Omega,$$

$$= 360 + 240 = \underline{600\ \Omega.}$$

(*b*) For the tee attenuator, the resistor values are given by

$$R_1 = R_0\frac{(n-1)}{(n+1)} \qquad R_2 = \frac{2nR_0}{n^2-1},$$

where n is the attenuation factor.
Using the equation for R_1,

$$R_1 = R_0\frac{(n-1)}{(n+1)}.$$

$$\therefore \quad R_1(n+1) = R_0(n-1).$$

$$\therefore \quad nR_1 + R_1 = nR_0 - R_0.$$

$$\therefore \quad R_1 + R_0 = nR_0 - nR_1.$$

$$\therefore \quad n = \frac{R_0 + R_1}{R_0 - R_1} = \frac{600 + 360}{600 - 360} = 4.$$

Attenuation $= 20 \log n = 20 \log 4 = \underline{12{\cdot}04\,\text{dB}}.$

(*c*)

When the loaded attenuator is connected to the signal generator, a resistance of 600 Ω appears at its terminals. This has the effect of voltage dividing the generator EMF between the generator internal resistance and the load. Since the generator is matched to the load, only one half of the EMF appears at the generator terminals.

The potential difference across the load is given by

$$V_L = \frac{E}{2} \times \frac{1}{n} = \frac{10}{2} \times \frac{1}{4} = 1{\cdot}25\,\text{V}.$$

The overall attenuation is given by $2n$, since half of the potential difference is lost inside the generator.

$$\therefore \quad \text{Loss} = 20 \log 2n = 20 \log(2 \times 4) = 20 \log 8 = \underline{18{\cdot}06\,\text{dB}}.$$

Note that 50% loss occurs because of the generator. Since this is equivalent to 6 dB, the same result could be obtained by adding 6 dB to the loss in the attenuator.

Q8 *Figure 4 shows the basic circuit of a Schering bridge which is used to measure the parameters of a high voltage transmission line.* C_x *and* r_x *represent the capacity and its series loss resistance of the line.*

(*a*) *Show that under the condition of balance the bridge is not frequency dependent.*

(*b*) *During a test on a 135 kV 50 Hz line, balance is obtained when the bridge variables are 620 nF and 112 Ω. The standard components are 470 nF and 56 Ω.*

Find (*i*) *the line parameters,*
(*ii*) *the power loss, and*
(*iii*) *percentage power wastage when the load on the line is 200 A.*

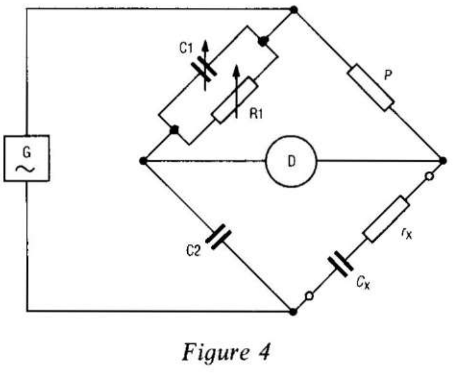


Figure 4

A8

In the derivation of the equations for the unknown parameters, it is worthwhile to spend a little time setting up the equations for each arm before inserting the values into the balance equation. This makes the analysis much more straightforward. Call the impedance of each arm Z_1, Z_2, etc., these being taken in sequence either clockwise or anticlockwise. Since balance occurs when the products of opposite arms are equal, the balance equation will always be

$$Z_1Z_3 = Z_2Z_4.$$

Let $Z_1 = P$, then

$$Z_2 = r_x + \frac{1}{j\omega C_x} = \frac{1 + j\omega C_x r_x}{j\omega C_x},$$

and

$$Z_3 = \frac{1}{j\omega C_2}.$$

By the product over sum rule,

$$Z_4 = \frac{R_1\left(\dfrac{1}{j\omega C_1}\right)}{R_1 + \dfrac{1}{j\omega C_1}}.$$

Multiplying both denominator and numerator by $j\omega C_1$ gives

$$Z_4 = \frac{R_1}{1 + j\omega C_1 R_1}.$$

At balance, $Z_1Z_3 = Z_2Z_4$.

$$\therefore \quad P\left(\frac{1}{j\omega C_2}\right) = \left(\frac{1 + j\omega C_x r_x}{j\omega C_x}\right)\left(\frac{R_1}{1 + j\omega C_1 R_1}\right).$$

Cross multiplying,

$$Pj\omega C_x(1 + j\omega C_1 R_1) = j\omega C_2 R_1(1 + j\omega C_x r_x).$$

Expanding the terms,

$$j\omega C_x P + j^2\omega^2 C_1 R_1 C_x P = j\omega C_2 R_1 + j^2\omega^2 C_x C_2 R_1 r_x.$$

Since $j^2 = -1$,

$$j\omega C_x P - \omega^2 C_1 R_1 C_X P = j\omega C_2 R_1 - \omega^2 C_x C_2 R_1 r_x.$$

Equating imaginary terms,

$$j\omega C_x P = j\omega C_2 R_1.$$

$$\therefore \quad C_x = \frac{C_2 R_1}{P}.$$

Equating real terms,

$$\omega^2 C_1 R_1 C_x P = \omega^2 C_x C_2 R_1 r_x.$$

$$\therefore \quad r_x = \frac{C_1 P}{C_2}.$$

Since neither of the balance equations feature ω or f, the bridge at balance is not frequency dependent.

(*b*) (*i*)

$$C_x = \frac{C_2 R_1}{P} = \frac{470 \times 10^{-9} \times 112}{56}\ \text{F} = \underline{940\ \text{nF}.}$$

$$r_x = \frac{C_1 P}{C_2} = \frac{620 \times 10^{-9} \times 56}{470 \times 10^{-9}}\ \Omega = \underline{73{\cdot}87\ \Omega.}$$

To calculate the power loss, it is simplest to find the current which flows in the series $C_x r_x$ circuit and then find $I^2 r_x$.

(*ii*) $$X_c = \frac{1}{2\pi f C}.$$

At 50 Hz

$$X_c = \frac{1}{2\pi \times 50 \times 940 \times 10^{-9}} = 3386.3\ \Omega.$$

$$Z = \sqrt{(r_x^2 + X_{Cx}^2)} = \sqrt{(73{\cdot}87^2 + 3386{\cdot}3^2)} = 3387\ \Omega.$$

At 135 kV,

$$I = \frac{135 \times 10^3}{3387} = 39{\cdot}86\ \text{A}.$$

The power loss is given by $I^2 r_x$

$$= 39{\cdot}86^2 \times 73{\cdot}87\ \text{W} = \underline{117{\cdot}37\ \text{kW}.}$$

(*iii*) When the load is 200 A, the output power is

$$P_o = VI = 135 \times 10^3 \times 200 = 27 \times 10^6\ \text{W} = 27\ \text{MW}.$$

$$\text{Power wastage} = \frac{117{\cdot}37 \times 10^3}{27 \times 10^6} \times 100\% = \underline{0{\cdot}435\%.}$$

PART 2—Electronics IV (BTEC)

Q9 Figure 5 shows an amplifier of intrinsic voltage gain 40 dB, whose losses are represented by a series resistor–capacitor network connected to the amplifier output. v_x *is the network input.*

(*a*) *Calculate the voltage gain in decibels when the input signal has a frequency of 80 kHz.*
(*b*) *Find the corner frequency of the amplifier.*
(*c*) *Calculate the transition frequency for the amplifier circuit.*
(*d*) *Sketch the amplifier characteristic.*
(*e*) *Calculate the output power dissipated in an external load of 10 kΩ when an input signal of 10·2 mV DC is applied at the input to the circuit.*

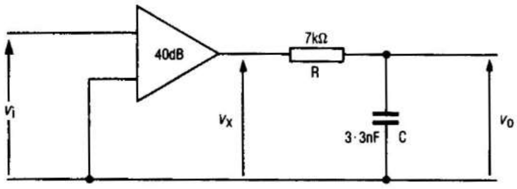


Figure 5

A9

When an AC signal is applied, although no loss occurs within the intrinsic amplifier, the CR network forms a voltage divider. The result is that, as the frequency increases, since the capacitive reactance falls, the output voltage has a decreasing value. The network loss can be calculated as follows:

By voltage division, $$\frac{v_o}{v_x} = \frac{\dfrac{1}{j\omega C}}{R + \dfrac{1}{j\omega C}}.$$

Multiplying numerator and denominator by $j\omega C$, and rearranging,

$$\frac{v_o}{v_x} = \frac{1}{1 + j\omega CR}.$$

$$\therefore \quad \left|\frac{v_o}{v_x}\right| = \frac{1}{\sqrt{\{1 + (\omega CR)^2\}}}.$$

(*a*) $$\frac{v_o}{v_x} = \frac{1}{1 + j\omega CR} = \frac{1}{1 + j2\pi \times 80 \times 10^3 \times 3{\cdot}3 \times 10^{-9} \times 7000} = \frac{1}{1 + j11{\cdot}61}.$$

$$\therefore \quad \left|\frac{v_o}{v_x}\right| = \frac{1}{\sqrt{(1 + 11{\cdot}61^2)}} = \frac{1}{11{\cdot}65} = 0{\cdot}0858.$$

The voltage gain of the intrinsic amplifier can be found as follows:

$$\text{gain} = 20 \log \frac{v_x}{v_i} \text{ dB}.$$

$$\therefore \quad \frac{\text{gain in dB}}{20} = \log \frac{v_x}{v_i}.$$

Taking the antilogarithm of both sides,

$$\frac{v_x}{v_i} = 10^{\text{gain}/20}.$$

$$\frac{v_x}{v_i} = 10^{\text{gain}/20} = 10^{40/20} = 10^2 = 100.$$

$$\frac{v_o}{v_i} = \frac{v_x}{v_i} \times \frac{v_o}{v_x} = 100 \times 0{\cdot}0858 = 8{\cdot}58.$$

$$\text{Gain} = 20 \log \frac{v_o}{v_i} = 20 \log 8{\cdot}58 = \underline{18{\cdot}67\text{ dB}}.$$

The corner frequency is that input signal frequency which produces an output 3 dB down on the low-frequency voltage gain; that is, when the output is reduced by a factor of $1/\sqrt{2}$. Since all the losses occur in the network, the 3 dB frequency is reached when

$$\frac{1}{1 + \mathrm{j}\omega CR} = \frac{1}{1 + \mathrm{j}1}.$$

That is,

$$\left|\frac{1}{1 + \mathrm{j}1}\right| = \frac{1}{\sqrt{(1+1)}} = \frac{1}{\sqrt{2}}.$$

(*b*) When $\omega CR = 1$, $\omega = \dfrac{1}{CR}$

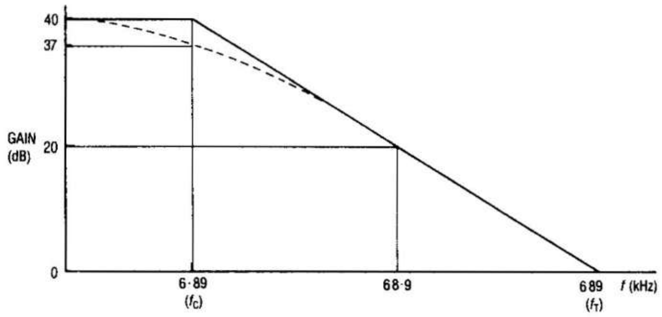
$$\therefore \quad f_c = \frac{1}{2\pi CR} = \frac{1}{2\pi \times 3{\cdot}3 \times 10^{-9} \times 7000} = \underline{6890\text{ Hz}}.$$

(*c*)

For the CR network, beyond the 3 dB frequency, the fall-off rapidly assumes a value of 20 dB per decade. When a fall-off of 40 dB is reached for this circuit, the gain will be 0 dB (unity voltage gain). At this frequency, the gain in decibels goes from a positive to a negative value and is thus called the *transition frequency* (f_T). For each reduction of 20 dB, the frequency is multiplied by a factor of 10.

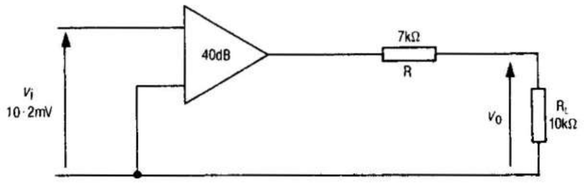
$$f_T = f_c \times 10^{\text{gain}/20} = 6890 \times 10^{40/20} = 6890 \times 100 = \underline{689\text{ kHz}}.$$

(*d*)



When a DC input signal is applied, the CR network produces no loss, but the presence of an external resistive load produces voltage division.

(*e*)



$$\frac{v_o}{v_i} = 10^{40/20} \times \frac{10}{10 + 7} = 100 \times \frac{10}{17} = 58{\cdot}82.$$

$$\therefore \quad v_o = 58{\cdot}82 v_i = 58{\cdot}82 \times 10{\cdot}2 \times 10^{-3} = 0{\cdot}6\text{ V}.$$

$$\text{Output power} = \frac{v_o^2}{R_L} = \frac{0{\cdot}6^2}{10 \times 10^3} = \underline{36\ \mu\text{W}}.$$

Q10 *Figure 6 shows the circuit of a transistor amplifier to which negative feedback is applied by not using a capacitor to decouple the emitter resistor.*

(*a*) *Draw the h parameter equivalent circuit, making the assumption that* h_{re} *and* h_{oe} *are insignificant when the circuit is operated with a small input signal at midband frequency.*
(*b*) *Derive an expression for the output voltage and show that the transistor input voltage is given by*

$$v_i = i_i\{h_{ie} + (1 + h_{fe})R_E\}.$$

(*c*) *Using the results obtained in part* (*b*), *find the voltage gain when*

$$R_L = 3300\,\Omega \qquad R_E = 180\,\Omega$$

$$h_{ie} = 960\,\Omega \qquad h_{fe} = 120$$

(*d*) *Calculate the voltage gain with negative feedback using the relationship*

$$A'_v = \frac{A_v}{1 + \beta A_v},$$

and compare the result with that obtained in part (*c*).
(*e*) *Calculate the input impedance for the complete circuit.*

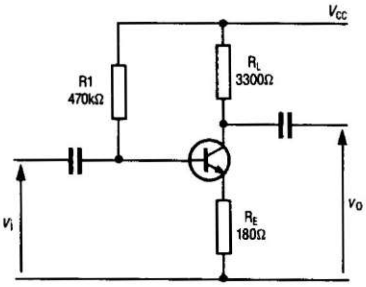
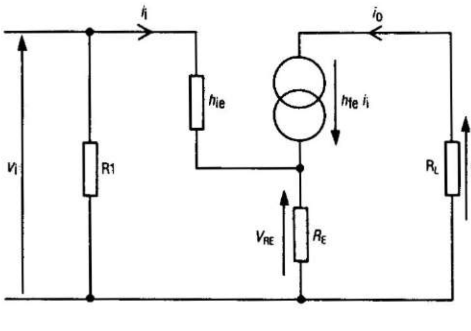


Figure 6

A10 (*a*)



(*b*) The current i_o flows through resistor R_L from bottom to top in the diagram.

$$\therefore \quad v_o = -i_o R_L = -h_{fe} i_i R_L.$$

The input voltage is given by

$$v_i = h_{ie} i_i + v_{R_E}$$

But,

$$v_{R_E} = (i_i + h_{fe} i_i) R_E = i_i(1 + h_{fe}) R_E.$$

$$\therefore \quad v_i = h_{ie} i_i + i_i(1 + h_{fe}) R_E = i_i\{h_{ie} + (1 + h_{fe}) R_E\}.$$

(*c*) The voltage gain is given by v_o/v_i.

$$\frac{v_o}{v_i} = \frac{-h_{fe} i_i R_L}{i_i\{h_{ie} + (1 + h_{fe}) R_E\}}.$$

Eliminating i_i,

$$\frac{v_o}{v_i} = A'_v = -\frac{h_{fe}R_L}{h_{ie} + (1 + h_{fe})R_E}.$$

Inserting values

$$A'_v = -\frac{120 \times 3300}{960 + (1 + 120)180} = \underline{-17{\cdot}414.}$$

(*d*) Using the equation for voltage gain with no feedback,

$$A_v = -\frac{h_{fe}R_L}{h_{ie}} = -\frac{120 \times 3300}{960} = -412{\cdot}5.$$

Since $R_L \gg R_E$, $\beta = \dfrac{R_E}{R_L} = \dfrac{180}{3300}$.

Using the equation

$$A'_v = \frac{A_v}{1 + \beta A_v} = -\frac{412{\cdot}5}{1 + \left(\dfrac{180}{3300} \times 412{\cdot}5\right)} = \underline{-17{\cdot}55.}$$

The error between the two values is given by

$$\frac{17{\cdot}414 - 17{\cdot}55}{17{\cdot}414} \times 100\% = \underline{0{\cdot}8\%.}$$

It is worthwhile to consider why the error occurs; the value of β is originally obtained by taking the potential difference across resistor R_E compared with that across resistor R_L based on the idea that both resistors carry the same current. In fact, resistor R_E carried one 'lot' of base current more than the collector resistor because $I_E = I_B + I_C$ for the DC case and $i_e = i_b + h_{fe}i_b$ for the AC case.

When the expression for voltage gain is changed to

$$A'_v = -\frac{h_{fe}R_L}{h_{ie} + h_{fe}R_E},$$

then

$$A'_v = -\frac{120 \times 3300}{960 + (120 \times 180)} = -17{\cdot}55,$$

which is the identical value.

In practice, the small error produced is outweighed by the percentage error in the components.

(*e*) From $v_i = i_i\{h_{ie} + (1 + h_{fe})R_E\}$,

$$\frac{v_i}{i_i} = Z'_i = h_{ie} + (1 + h_{fe})R_E.$$

Inserting values,

$$Z'_i = 960 + (1 + 120)180 = 22\,740\,\Omega.$$

The circuit input impedance is Z'_i in parallel with the base bias resistor

$$= Z'_i /\!/ R_1 = \frac{22\,740 \times 470\,000}{22\,740 + 470\,000} = \underline{21{\cdot}69\text{ k}\Omega.}$$

Q11 *A non-inverting small signal voltage amplifier has a voltage gain of 250 at 83 Hz, at which frequency the interstage coupling circuits produce an overall phase shift of 40°.*

Calculate the overall voltage gain and phase shift at 83 Hz when 2% of the output signal is applied to the input as negative feedback.

A11 At 83 Hz, $A_v = 250 \angle 40°$.

Using the feedback equation,

$$A'_v = \frac{A_v}{1 + \beta A_v} = \frac{250 \angle 40°}{1 + \left(\dfrac{2}{100} \times 250 \angle 40°\right)} = \frac{250 \angle 40°}{1 + 5 \angle 40°}.$$

Converting $5 \angle 40°$ to $(a + jb)$ form using the relationship $r \angle \theta = r\cos\theta + jr\sin\theta$,

$$5 \angle 40° = 5\cos 40° + j5\sin 40° = 3{\cdot}83 + j3{\cdot}21.$$

$$\therefore \quad A'_v = \frac{250 \angle 40°}{1 + 3{\cdot}83 + j3{\cdot}21} = \frac{250 \angle 40°}{4{\cdot}83 + j3{\cdot}21}.$$

Now, reconverting the denominator using

$$a + jb \equiv \sqrt{(a^2 + b^2)} \angle \tan^{-1}\frac{b}{a}.$$

$$4{\cdot}83 + j3{\cdot}21 = \sqrt{(4{\cdot}83^2 + 3{\cdot}21^2)} \angle \tan^{-1}\frac{3{\cdot}21}{4{\cdot}83} = 5{\cdot}8 \angle 33{\cdot}6°.$$

$$\therefore \quad A'_v = \frac{250 \angle 40°}{5{\cdot}8 \angle 33{\cdot}6°} = \frac{250}{5{\cdot}8} \angle (40° - 33{\cdot}6°) = \underline{43{\cdot}1 \angle 6{\cdot}4°.}$$

Q12 *Figure 7 shows a rectifier circuit which consists of a thyristor and a load resistor of 40 Ω. The input to the circuit is 240 V at mains frequency.*

Calculate

(a) the mean voltage which can be measured across the load resistor, and

(b) the power dissipation in the load.

When the firing angle for the thyristor is 62°.

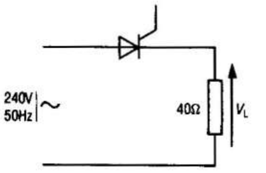
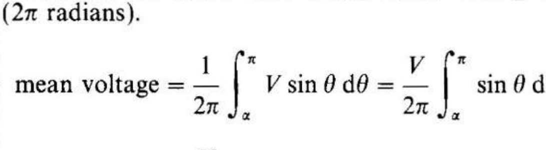


Figure 7

A12



The mean voltage is found by integrating the wave between α and π radians, the result then being taken during the complete cycle (2π radians).

$$\text{mean voltage} = \frac{1}{2\pi}\int_{\alpha}^{\pi} V\sin\theta \, d\theta = \frac{V}{2\pi}\int_{\alpha}^{\pi}\sin\theta \, d\theta = \frac{V}{2\pi}[-\cos\theta]_{\alpha}^{\pi}$$

$$= \frac{V}{2\pi}\{(-\cos\pi) - (-\cos\alpha)\}.$$

But $-\cos\pi = +1$,

$$\therefore \quad \text{mean voltage} = \frac{V}{2\pi}(1 + \cos\alpha).$$

(*a*) The potential difference measured across the load resistor is given by

$$\text{mean voltage} = \frac{V}{2\pi}(1 + \cos\alpha) = \frac{240\sqrt{2}}{2\pi}(1 + \cos 62^\circ) = \underline{79{\cdot}38 \text{ volts.}}$$

The RMS voltage is required to calculate the load power dissipation. This is found as follows:

$$\text{Mean squared voltage} = \frac{1}{2\pi}\int_\alpha^\pi (V\sin\theta)^2\,\mathrm{d}\theta = \frac{V^2}{2\pi}\int_\alpha^\pi \sin^2\theta\,\mathrm{d}\theta.$$

Using the substitution $\sin^2\theta = \frac{1}{2}(1 - \cos 2\theta)$,

$$\text{mean squared voltage} = \frac{V^2}{4\pi}\int_\alpha^\pi (1 - \cos 2\theta)\,\mathrm{d}\theta = \frac{V^2}{4\pi}\left[\theta - \frac{\sin 2\theta}{2}\right]_\alpha^\pi.$$

$$\therefore \quad \text{mean squared voltage} = \frac{V^2}{4\pi}\left\{(\pi - \alpha) - \left(\frac{\sin 2\pi}{2} - \frac{\sin 2\alpha}{2}\right)\right\}.$$

But $\sin 2\pi = 0$

$$\therefore \quad \text{mean squared voltage} = \frac{V^2}{4\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right).$$

$$\therefore \quad V_{\text{RMS}} = \sqrt{\left\{\frac{V^2}{4\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right\}},$$

$$= \frac{V}{2}\sqrt{\left\{\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right\}}.$$

In the above expression care must be taken to insert α as radians *not* degrees.

(*b*)

$$V_{\text{RMS}} = \frac{V}{2}\sqrt{\left\{\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right\}},$$

and $62^\circ \equiv \frac{\pi}{180} \times 62$ radians $\equiv 1{\cdot}082$ radians.

$$\therefore \quad V_{\text{RMS}} = \frac{240\sqrt{2}}{2}\sqrt{\left\{\frac{1}{\pi}\left(\pi - 1{\cdot}082 + \frac{\sin 2 \times 62^\circ}{2}\right)\right\}} = \frac{240\sqrt{2}}{2}\sqrt{\left(\frac{1}{\pi} \times 2{\cdot}474\right)}$$

$$= 150{\cdot}6 \text{ volts.}$$

The power dissipated in the load

$$= \frac{V_{\text{RMS}}^2}{R_{\text{L}}} = \frac{150{\cdot}6^2}{40} = \underline{567\text{ W.}}$$

Q13 *An output transistor is coupled to a resistive 15 Ω load by a step-down transformer of ratio 20:1. Under static conditions of class A bias, the collector current is 22 mA.*

When an input signal is applied to the base of the transistor, the collector current is related to the input voltage by the expression

$$i_{\text{C}} = 122v_{\text{i}} + 170v_{\text{i}}^2 + I_{\text{C,STAT}}\,\text{mA}.$$

(*a*) *Obtain an expression for the collector current when the input signal is 85 mV, 1000 Hz and show that second harmonic distortion is produced.*

(*b*) *Calculate the percentage harmonic distortion in the*

(*i*) *collector current, and*
(*ii*) *output power.*

(*c*) *In the presence of the input signal, what is the average value of the collector current?*
(*d*) *Sketch the collector current waveform.*
(*e*) *Calculate the power dissipated in the load.*

A13

> The input signal must be expressed in the general form of $v = V \sin \omega t$, where V is the signal amplitude and ω is the angular frequency.

(*a*) Writing $V = 85\sqrt{2} \times 10^{-3}$ volts and $\omega = 2\pi \times 1000$ rad s^{-1}

$$v_i = 85\sqrt{2} \times 10^{-3} \sin 2000\pi t \text{ volts.}$$

$$\therefore \quad i_C = 122 \times 85\sqrt{2} \times 10^{-3} \sin 2000\pi t + 170(85\sqrt{2} \times 10^{-3} \sin 2000\pi t)^2 + 22,$$

$$= 14{\cdot}67 \sin 2000\pi t + 2{\cdot}46 \sin^2 2000\pi t + 22 \text{ mA.}$$

Using the substitution $\sin^2 \theta = \frac{1}{2}(1 - \cos 2\theta)$,

$$i_C = 14{\cdot}67 \sin 2000\pi t + \frac{2{\cdot}46}{2}(1 - \cos 4000\pi t) + 22,$$

$$\underline{= 14{\cdot}67 \sin 2000\pi t + 1{\cdot}23 - 1{\cdot}23 \cos 4000\pi t + 22 \text{ mA.}}$$

The cosine term can be seen to be at 2000 Hz which is twice the frequency of the applied signal so that second harmonic distortion has been produced by the square law characteristic of the transistor.

(*b*) (*i*) Comparing the amplitude of the fundamental and second harmonic components

$$\text{second harmonic distortion in collector current} = \frac{1{\cdot}23}{14{\cdot}67} \times 100\% = \underline{8{\cdot}38\%.}$$

(*ii*) The output power is proportional to the square of the current (I^2R watts) so that

$$\text{second harmonic distortion in output power} = \left(\frac{1{\cdot}23}{14{\cdot}67}\right)^2 \times 100\% = \underline{0{\cdot}7\%.}$$

(*c*)

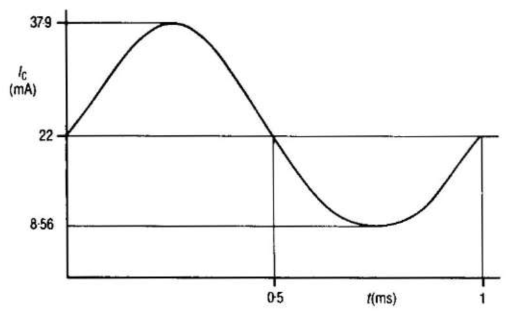
> When the input signal is applied, an additional DC component of collector current is produced, as seen by the expression in part (*a*).

Average collector current when the input signal is applied

$$= I_{C,STAT} + \text{extra component} = 22 + 1{\cdot}23 = \underline{23{\cdot}23 \text{ mA.}}$$

(*d*) Maximum collector current $= 14{\cdot}67 + 1{\cdot}23 + 22 = 37{\cdot}9$ mA.

Minimum collector current $= -14{\cdot}67 + 1{\cdot}23 + 22 = 8{\cdot}56$ mA.



(*e*) The RMS value of the collector current, which will be transferred to the transformer secondary is given by

$$= \frac{1}{\sqrt{2}}\sqrt{\{I_F^2 + I_{2H}^2\}} = \frac{1}{\sqrt{2}}\sqrt{\{14{\cdot}67^2 + 1{\cdot}23^2\}} = 10{\cdot}41 \text{ mA.}$$

In the secondary circuit,

$$I_R = 10{\cdot}41 \times 10^{-3} \times 20 = 208{\cdot}2 \text{ mA}$$

$$\text{Power dissipated in the load} = I_R^2 R = 0{\cdot}2082^2 \times 15 = \underline{0{\cdot}65 \text{ W.}}$$

Q14 Figure 8 shows the circuit of a relay controller where the relay is energised by the operation of a push switch. A silicon transistor is used and when collector current flows the base current is 45 μA. The large signal current gain of the transistor is 36.

(a) Find a suitable value of R_1.

(b) Given that the DC resistance of the relay coil is 1400 Ω, calculate a suitable value of R_3 *which will bring the collector potential difference into saturation.*

(c) Under a certain fault condition, the base connection becomes disconnected inside the transistor. Calculate the potential difference at the base when the switch is operated.

(d) If a 1000 Ω/V meter were used on the 10 V full-scale deflection range, what potential difference will be measured for the condition given in part (c)?

(e) Calculate the potential difference at the collector when the switch is closed, assuming that the collector current falls exponentially.

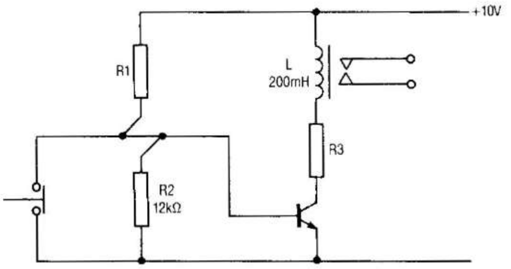


Figure 8

A14

Under saturation conditions for the silicon transistor,

$$V_{\mathrm{BE,SAT}} = 0{\cdot}8 \text{ volts} \qquad V_{\mathrm{CE,SAT}} = 0{\cdot}2 \text{ volts.}$$

(*a*)

$$I_{\mathrm{R2}} = \frac{V_{\mathrm{BE,SAT}}}{R_2} = \frac{0{\cdot}8}{12 \times 10^3}\,\mathrm{A} = 66{\cdot}7\,\mu\mathrm{A}.$$

$$I_{\mathrm{R1}} = I_{\mathrm{R2}} + I_{\mathrm{B}} = 66{\cdot}7 + 45 = 111{\cdot}7\,\mu\mathrm{A}.$$

$$R_1 = \frac{V_{\mathrm{CC}} - V_{\mathrm{BE,SAT}}}{I_{\mathrm{R1}}} = \frac{10 - 0{\cdot}8}{111{\cdot}7 \times 10^{-6}}\,\Omega = \underline{82{\cdot}36\,\mathrm{k\Omega}.}$$

(*b*)

$$I_{\mathrm{C}} = h_{\mathrm{FE}} I_{\mathrm{B}} = 36 \times 45 \times 10^{-6}\,\mathrm{A} = 1{\cdot}62\,\mathrm{mA}.$$

$$r + R_3 = \frac{V_{\mathrm{CC}} - V_{\mathrm{CE,SAT}}}{I_{\mathrm{C}}} = \frac{10 - 0{\cdot}2}{1{\cdot}62 \times 10^{-3}} = 6049\,\Omega.$$

$$\therefore \quad R_3 = 6049 - r = 6049 - 1400\,\Omega = \underline{4649\,\Omega.}$$

The values of R_1 and R_3 fall conveniently close to preferred values so practical values of $R_1 = 82\,\mathrm{k\Omega}$ and $R_3 = 4{\cdot}7\,\mathrm{k\Omega}$ can be used.

(*c*) When the base connection of the transistor is open circuit, the base voltage can be found by voltage division.

$$\therefore \quad V_{\mathrm{B}} = V_{\mathrm{CC}} \frac{R_2}{R_1 + R_2} = 10 \frac{12}{82 + 12} = \underline{1{\cdot}277\,\mathrm{V}.}$$

(*d*) When the meter is connected across resistor R2, resistor R2 is shunted by a 10 kΩ resistance

$$\therefore \quad R_2 /\!/ R_{\mathrm{m}} = \frac{12 \times 10}{12 + 10}\,\mathrm{k\Omega} = \underline{5{\cdot}455\,\mathrm{k\Omega}.}$$

$$V_{\mathrm{B}} = \frac{5{\cdot}455}{82 + 5{\cdot}455} \times 10 = \underline{0{\cdot}62\,\mathrm{V}.}$$

The foregoing shows that by the incorrect selection of a test meter and possible careless reading of the indicated value, the impression may be gained that the fault does not lie in the transistor base circuit. It is worthwhile to realise that small variations in potentials at the base can result in very different operating conditions in the circuit.

(*e*)

The EMF produced across the inductor, when the switch is closed is given by

$$e = -L\frac{di}{dt},$$

and since the collector current falls exponentially,

$$i = Ie^{-t/\tau}.$$

Differentiating this expression,

$$\frac{di}{dt} = -\frac{1}{\tau}Ie^{-t/\tau} = -\frac{I}{\tau}e^{-t/\tau}.$$

At the instant of closing the switch, $t = 0$.

$$\therefore \quad \frac{di}{dt} = -\frac{I_C}{\tau}e^0 = -\frac{I_C}{\tau}.$$

For the inductive circuit

$$\tau = \frac{L}{r + R_3} = \frac{200 \times 10^{-3}}{6049}\text{ s.}$$

$$\therefore \quad \frac{I_C}{\tau} = \frac{1{\cdot}62 \times 10^{-3} \times 6049}{200 \times 10^{-3}} = 49\text{ A s}^{-1}$$

Since $e = -L\dfrac{di}{dt}$,

$$e = -200 \times 10^{-3} \times (-49) = 9{\cdot}8\text{ V}$$

The polarity of the induced EMF is such that it adds to V_{CC}. Thus the collector potential difference when the switch is closed is given by

$$V_{CC} + e = 10 + 9{\cdot}8 = \underline{19{\cdot}8\text{ V}}.$$

Q15 *Figure 9 shows an ideal operational amplifier connected in inverting mode with its associated input and feedback components. The external load is a pure resistor of 2·2 kΩ.*

(*a*) *Obtain an expression for the overall voltage gain.*
(*b*) *Calculate the voltage gain for a*

(*i*) *DC input signal*
(*ii*) *1000 Hz input signal.*

(*c*) *Calculate the input signal required to produce a dissipation of 400 mW at 1000 Hz, in the external load.*

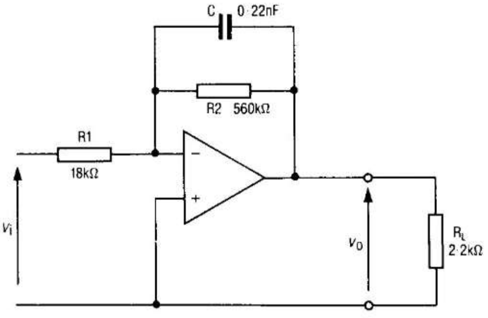


Figure 9

A15 (*a*) The voltage gain is given by

$$A_v = -\frac{Z_f}{Z_i},$$

where Z_f is the parallel combination of C and R_2.

Using the product-over-sum rule

$$Z_f = \frac{R_2 \dfrac{1}{j\omega C}}{R_2 + \dfrac{1}{j\omega C}} = \frac{R_2}{1 + j\omega CR_2}.$$

$$\therefore \quad A_v = -\frac{1}{R_1}\left(\frac{R_2}{1 + j\omega CR_2}\right) = -\frac{R_2}{R_1}\left(\frac{1}{1 + j\omega CR_2}\right).$$

(*b*) (*i*) When the input signal is a direct voltage, $\omega CR = 0$.

$$\therefore \quad A_v = -\frac{R_2}{R_1}$$

Inserting values

$$A_v = -\frac{560 \times 10^3}{18 \times 10^3} = -31{\cdot}1.$$

(*ii*) At 1000 Hz,

$$A_v = -31{\cdot}1\left(\frac{1}{1 + j2\pi 1000 \times 0{\cdot}22 \times 10^{-9} \times 560 \times 10^3}\right) = -31{\cdot}1 \times \frac{1}{1 + j0{\cdot}774}.$$

$$1 + j0{\cdot}774 \equiv \sqrt{(1 + 0{\cdot}774^2)} \angle \tan^{-1}\frac{0{\cdot}774}{1} = 1{\cdot}265 \angle 37{\cdot}74^\circ.$$

$$\therefore \quad A_v = \frac{-31{\cdot}1}{1{\cdot}265 \angle 37{\cdot}74^\circ}$$

The minus sign signifies a phase shift of 180° when the input is sinusoidal.

$$\therefore \quad A_v = \frac{31{\cdot}1 \angle 180^\circ}{1{\cdot}265 \angle 37{\cdot}74^\circ} = \frac{31{\cdot}1}{1{\cdot}265} \angle(180^\circ - 37{\cdot}74^\circ) = 24{\cdot}58 \angle 142{\cdot}26^\circ.$$

(*c*) The load power is given by

$$P = \frac{V_0^2}{R_L}.$$

$$\therefore \quad V_0 = \sqrt{(PR_L)} = \sqrt{(400 \times 10^{-3} \times 2{\cdot}2 \times 10^3)} = 29{\cdot}7\ \text{V}.$$

$$V_i = \frac{V_0}{|A_v|} = \frac{29{\cdot}7}{24{\cdot}58} = 1{\cdot}21\ \text{V}.$$

Q16 *The circuit shown in Figure 10 is used to reject the note C above middle C (524 Hz) from the output of an audio amplifier. At midband frequency, the voltage gain is -112. The effective resistance of the inductor is 20 Ω and the emitter capacitor is 680 nF.*

(*a*) *Calculate the pre-set value of the inductor.*
(*b*) *Find the tuned circuit dynamic impedance.*
(*c*) *Calculate the rejection ratio of the circuit at 524 Hz. Express the rejection in decibels.*

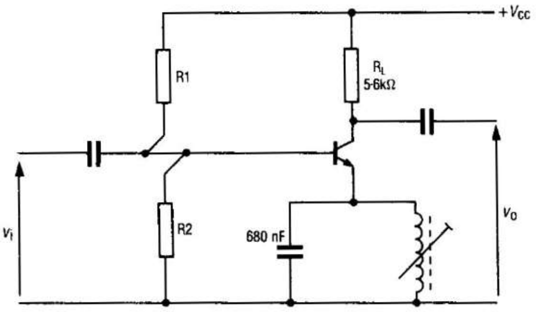


Figure 10

A16 (*a*) At the frequency of resonance, $\omega L = \dfrac{1}{\omega C}$.

$$\therefore \quad L = \frac{1}{\omega^2 C} = \frac{1}{(2\pi \times 524)^2 \times 680 \times 10^{-9}} \text{ H} = \underline{135{\cdot}7 \text{ mH.}}$$

(*b*) The tuned circuit dynamic impedance

$$Z_D = \frac{L}{Cr} = \frac{135{\cdot}7 \times 10^{-3}}{680 \times 10^{-9} \times 20} = \underline{9978\ \Omega.}$$

(*c*)

When the tuned circuit is at the frequency of resonance (when the input signal is at a frequency of 524 Hz), it appears to be a pure resistance. This results in a large amount of negative feedback being applied to the amplifier.

The value of the emitter resistor is not small compared with R_L so the approximation $\beta = (R_E/R_L)$ cannot be used.

When $R_E \nless R_L$, $\beta = \dfrac{R_E}{R_E + R_L}$ where $R_E \equiv Z_D$.

$$\therefore \quad \beta = \frac{Z_D}{Z_D + R_L} = \frac{9978}{9978 + 5600} = 0{\cdot}64.$$

Using the feedback equation

$$A'_v = \frac{A_v}{1 + \beta A_v} = -\frac{112}{1 + (0{\cdot}64 \times 112)} = \underline{-1{\cdot}54.}$$

Part of the output signal appears at the emitter and, since $Z_D \nless R_L$, the voltage gain at the collector must be corrected by a factor of $R_L/(R_L + Z_D)$.

Correcting the voltage gain between v_i and v_o,

$$\frac{v_o}{v_i} = A'_v\left(\frac{R_L}{R_L + Z_D}\right) = -1{\cdot}54\left(\frac{5600}{5600 + 9978}\right) = -0{\cdot}55.$$

Rejection of the signal at 524 Hz compared with midband frequency is given by

$$20 \log \frac{A_v(\text{MB})}{A_v(524)} = 20 \log \frac{-112}{-0{\cdot}55} \text{ dB} = \underline{46.2 \text{ dB.}}$$

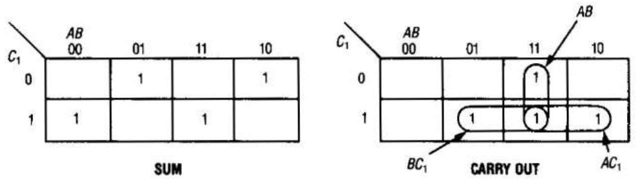
PART 3—Electronics (Digital) IV (BTEC)

Q17 *(a) Draw up the truth table for a full adder which gives* SUM *and* CARRY *outputs when the inputs are A, B, and a previously generated carry (C_1).*
(b) Show the SUM *and* CARRY *functions on Karnaugh maps.*
(c) Obtain the minimal form of the functions.
(d) Draw the logic circuits required to implement the full adder function.

A17 (*a*)

A	B	C_1	Sum, S	Carry, C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(*b*)



(*c*) From the Karnaugh map for the 'carry out' function,

$$C_0 = AB + AC_1 + BC_1.$$

Treating each group as a single term and applying De Morgan's theorem,

$$C_0 = \overline{\overline{AB}\,\overline{AC_1}\,\overline{BC_1}}.$$

This is now in NAND form and requires four gates.

The Karnaugh map for the SUM function does not lead to direct minimisation but an improvement can be effected.

$$S = \bar{A}\bar{B}C_1 + \bar{A}B\bar{C}_1 + ABC_1 + A\bar{B}\bar{C}_1.$$

Regrouping,

$$S = \bar{A}(\bar{B}C_1 + B\bar{C}_1) + A(BC_1 + \bar{B}\bar{C}_1)$$

Writing $\bar{B}C_1 + B\bar{C}_1$ as $B \oplus C_1$,

$$S = \bar{A}(B \oplus C_1) + A(BC_1 + \bar{B}\bar{C}_1).$$

By De Morgan's theorem,

$$BC_1 + \bar{B}\bar{C}_1 = \overline{(\bar{B} + \bar{C}_1)(B + C_1)},$$

$$= \overline{\bar{B}B + \bar{B}C_1 + \bar{C}_1B + \bar{C}_1C_1},$$

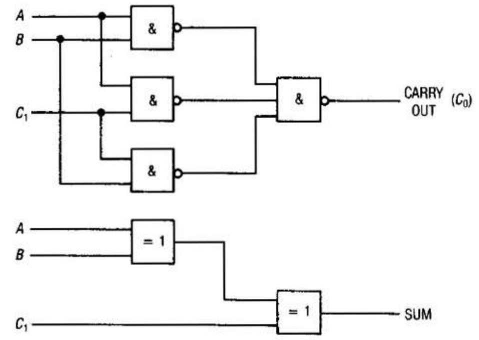
$$= \overline{\bar{B}C_1 + B\bar{C}_1} = \overline{B \oplus C_1}.$$

$$\therefore \quad S = \bar{A}(B \oplus C_1) + A(\overline{B \oplus C_1}).$$

$$\therefore \quad S = A \oplus B \oplus C_1.$$

This shows that the SUM function can be implemented with two EXCLUSIVE-OR gates.

(*d*)



Q18 *Figure 11 shows a digital-to-analogue converter which employs an operational amplifier and has four inputs.*

(*a*) *Calculate the output voltage obtained when the input nibble has a value of*

$$D_3D_2D_1D_0 = 1010,$$

when $0 \equiv 0$ *V,* $1 \equiv 4$ *V.*

(*b*) *Calculate the output voltage error when resistor R1 is 15% high in value.*

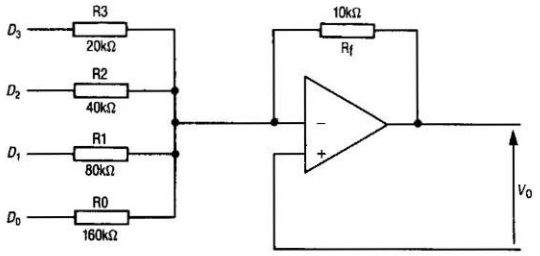


Figure 11

A18 (*a*) For the inverting operational amplifier,

$$v_o = -\frac{R_f}{R_i}v_i.$$

$$\therefore \quad V_o = -\left(\frac{R_f}{R_0}D_0 + \frac{R_f}{R_1}D_1 + \frac{R_f}{R_2}D_2 + \frac{R_f}{R_3}D_3\right),$$

$$= -\left(\frac{10}{160}\times 0 + \frac{10}{80}\times 4 + \frac{10}{40}\times 0 + \frac{10}{20}\times 4\right)\text{ V},$$

$$= -4\left(\frac{1}{8}+\frac{1}{2}\right)\text{ V} = \underline{-2{\cdot}5\text{ V.}}$$

(*b*) When R_1 is 15% high,

$$R_1 = 80 \times 10^3 \times 1{\cdot}15\,\Omega = 92\text{ k}\Omega.$$

$$\therefore \quad V_o = -4\left(\frac{10}{92}+\frac{10}{20}\right) = -2{\cdot}435\text{ V}.$$

$$\text{Therefore, the output error} = \frac{2{\cdot}5 - 2{\cdot}435}{2{\cdot}5}\times 100\% = \underline{2{\cdot}6\%.}$$

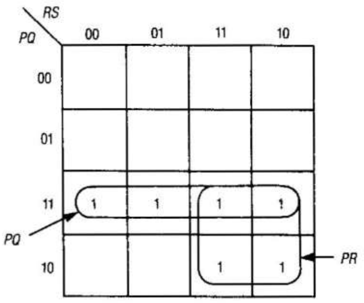
Q19 *A binary coded decimal counter counts from '0' to '9' after which it generates a carry for the next decade and then resets. In the event of a fault condition, it may produce an output not within the binary-coded decimal range.*

Design a combinational logic circuit in minimal form using NAND *gates which removes the clock pulse in the event of an unwanted output state. The four bistable outputs are P, Q, R, S where P is the most significant bit.*

A19

UNWANTED STATES

P	Q	R	S
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



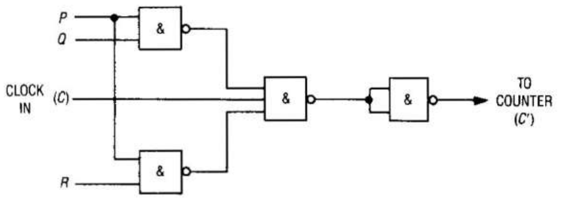
The Karnaugh map gives the unwanted function. Thus the clock pulse must reach the counter when the function is not present.

The clock pulse passed to the counter, C', is given by

$$C' = \overline{(PQ + PR)}C.$$

Converting the term in brackets to NAND form by the use of De Morgans theorem,

$$C' = (\overline{PQ})(\overline{PR})C.$$



Q20 *In order to demonstrate computer waveform generation, the following system was set up. Hexadecimal codes which are stored in a look-up table are accessed by a register which is incremented and decremented between 00 and 0B at time intervals of 50 μs. The data is then transferred to the input port of a digital-to-analogue converter (DAC) whose output produces* $\frac{255}{256} \times 10$ *V when the input is FF.*

The output of the DAC is then displayed on a cathode-ray oscilloscope (CRO) set to 'DC input'.

(*a*) *Draw up a table of the DAC output voltages given that the look-up table contains the following hexadecimal data.*

ADDRESS	*00*	*01*	*02*	*03*	*04*	*05*
DATA	*00*	*04*	*11*	*25*	*3F*	*5E*
ADDRESS	*06*	*07*	*08*	*09*	*0A*	*0B*
DATA	*A0*	*BF*	*D9*	*ED*	*FA*	*FF*

(*b*) *Draw the waveform which will be displayed on the CRO.*
(*c*) *Obtain the equation for the displayed waveform.*

A20 (*a*) Example calculation:
When the input to the DAC is 5E, the output is given by

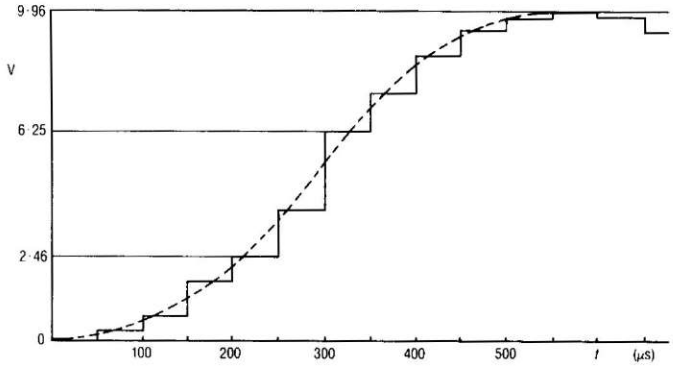
$$V_o = \frac{5\text{E}}{256} \times 10 \text{ volts.}$$

Converting to denary,

$$V_o = \frac{94}{256} \times 10 = 3{\cdot}67 \text{ V}.$$

ADDRESS	00	01	02	03	04	05
DATA	00	04	11	25	3F	5E
V_o (Volts)	0	0·156	0·66	1·45	2·46	3·67
ADDRESS	06	07	08	09	0A	0B
DATA	A0	BF	D9	ED	FA	FF
V_o (Volts)	6·25	7·46	8·48	9·26	9·77	9·96

(*b*)



(*c*) Inspection of the CRO waveform shows it to be of sinusoidal form, standing on zero volts, the maximum value reached being 9·96 V.

The complete cycle will have 22 steps, in which case the period,

$$T = 22 \times 50 \times 10^{-6} = 1{\cdot}1 \times 10^{-3}\ \text{s}.$$

The frequency, f, is given by

$$f = \frac{1}{T} = \frac{1}{1{\cdot}1 \times 10^{-3}} = 909\ \text{Hz}.$$

$$\omega = 2\pi f = 2\pi \times 909 = 1818\pi\ \text{rad s}^{-1}.$$

Further consideration shows the waveform to be a minus cosine wave of peak-to-peak value 9·96 V standing on a DC level of 9·96/2 V.

$$\therefore \quad V_o = \frac{9{\cdot}96}{2} + \left(-\frac{9{\cdot}96}{2}\cos 1818\pi t\right) = 4{\cdot}98 - 4{\cdot}98\cos 1818\pi t$$

$$= 4{\cdot}98(1 - \cos 1818\pi t)\ \text{V}.$$

> *Practical note*: In order to produce a more satisfactory curve, many more values need to be stored in the look-up table. In that case, the time interval will be reduced and the step size will give a much better approximation to the ideal curve.

Q21 *(a) Draw Karnaugh maps for the direct and inverse functions described by the Sigma notation*

$$F(WXYZ) = \sum 2, 6, 7, 8, 12, 13$$

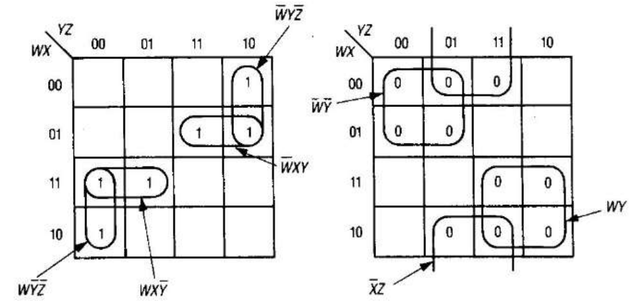
(b) Obtain the minimal expression in both cases.

(c) Draw the logic circuits using only NOR *gates.*

A21

> An explanation of the Sigma notation is given in the *Supplement to Br. Telecommun. Eng. J.* Vol. 7, Jan. 1989, Question 10.

(*a*)



DIRECT MAP INVERSE MAP

(*b*) From the direct map,

$$F = W\bar{Y}\bar{Z} + WX\bar{Y} + \bar{W}XY + \bar{W}Y\bar{Z}.$$

Using De Morgan's theorem on the separate groups,

$$F = \overline{(\bar{W} + Y + Z)} + \overline{(\bar{W} + \bar{X} + Y)} + \overline{(W + \bar{X} + \bar{Y})} + \overline{(W + \bar{Y} + Z)}.$$

From the inverse map,

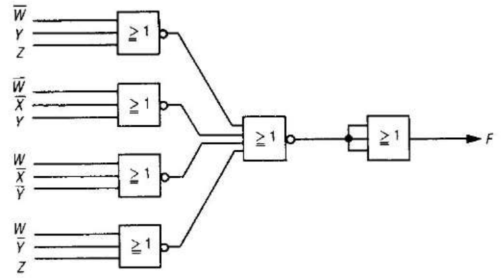
$$\bar{F} = \bar{W}\bar{Y} + \bar{X}Z + WY.$$

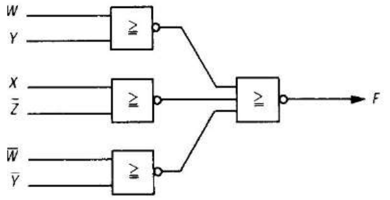
$$\therefore \quad F = \overline{\bar{W}\bar{Y} + \bar{X}Z + WY}.$$

Again using De Morgan's theorem on the separate groups

$$F = \overline{\overline{(W + Y)} + \overline{(X + \bar{Z})} + \overline{(\bar{W} + \bar{Y})}}$$

(*c*)





> This example has been chosen to illustrate the point that the implementation of the logic circuit may be more economical by the use of the inverse map. In this particular case, the direct map leads to six gates and 18 connections while the inverse map leads to only four gates and 10 connections.

Q22 *Figure 12 shows the basic arrangement of an analogue-to-digital converter. For the sake of simplification, the* RESET *facilities have been omitted. During the counting period, the comparator outputs a '1' until the ramp voltage reaches the value of the input voltage at which time the comparator outputs a '0'. The reference voltage to the ramp generator is held constant at −3·106 V by a zener diode.*

(*a*) *Given that v_i is always positive, find its value during the sampling period if, when the comparator outputs a '0', the counter which had previously been cleared holds $4B_H$.*

(*b*) *If the clock input frequency is reduced to 1 MHz, what will be the maximum input voltage which can be converted to a binary value?*

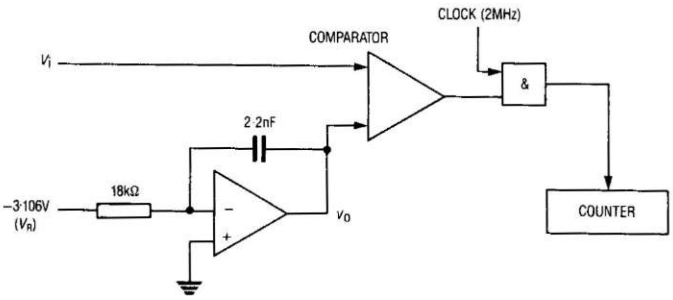


Figure 12

The ramp generator is an operational amplifier connected as an integrator, so its output is given by

$$v_o = -\frac{1}{CR}\int V_R \, dt,$$

where V_R is the constant voltage produced by the zener diode.

Solving the equation for v_o,

$$v_o = -\frac{V_R}{CR}\int dt = -\frac{V_R t}{CR} + K.$$

But, when $v_o = 0$ at $t = 0$,

$$v_o = -\frac{V_R t}{CR}$$

producing a linear ramp.

When v_o from the generator has the same value as the voltage being converted (v_i), the comparator outputs a '0' and counting ceases.

(*a*) By using the relationship $v_o = v_i = -\frac{V_R t}{CR}$, v_i can be obtained.

The period, $T = \frac{1}{f_{\text{clock}}} = \frac{1}{2 \times 10^{-6}} = 0{\cdot}5\ \mu\text{s}$.

Now, $4B_H \equiv 75$.

$$\therefore \quad t = 0{\cdot}5 \times 75 \times 10^{-6}\ \text{s} = 37{\cdot}5\ \mu\text{s}.$$

$$\therefore \quad v_i = \frac{-(-3{\cdot}106)37{\cdot}5 \times 10^{-6}}{18 \times 10^3 \times 2{\cdot}2 \times 10^{-9}} = \underline{2{\cdot}94\ \text{V}.}$$

(*b*) When the clock frequency is reduced to 1 MHz.

$$T = \frac{1}{f} = \frac{1}{10^6} = 1\ \mu\text{s}.$$

The hexadecimal value given in part (*a*) suggests a single byte (a double byte would be implied by $004B_H$) so the maximum count is FF.

$$FF \equiv 255.$$

$$\therefore \quad t = 255 \times 1 = 255\ \mu\text{s}.$$

$$\therefore \quad v_{i(\text{MAX})} = \frac{-(-3{\cdot}106)255 \times 10^{-6}}{18 \times 10^3 \times 2{\cdot}2 \times 10^{-9}} = \underline{20\ \text{V}.}$$

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